In the Specification:

Please amend the specification as follows:

At page 1, lines 15 - 21
BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the field of electronics amplifiers and more particularly to the field of signal conditioning circuits for signal boosting [[in]] within a predetermined bandwidth so as to compensate for reduced speaker performance resulting from reduced woofer size.

At page 2, lines 7 - 32:

In a first embodiment, the invention audio boost circuit has an input buffer responsive to a program input signal having high, low and mid-range frequency signal components for providing a buffered program signal. The buffered program signal is fed to an all pass phase inverter having an input coupled to receive the buffered program signal and an output providing an inverted buffered program signal, The buffered program signal is also fed to a band pass filter having a predetermined Q, responsive to the buffered program signal for providing an inverted band pass boosted program signal. A summing amplifier adds the inverted buffered program signal to the inverted band pass boosted program signal to provide a composite program [[signal]] signal as an output signal to a power amplifier and speaker combination. In a more particular embodiment, the band pass filter has a peak gain at a center frequency, and[[,]] a frequency adjustment means is provided for adjusting the frequency at which the peak gain occurs. In a [[yet]] more particular embodiment, the band pass filter has a first second and third resistor and a first and second capacitor[[,]]. [[and the]] The band pass filter's first, second and third resistor values and the values of the first and second capacitors are selected to obtain a Q in the range of from 3 to 6[[,]]. [[and [[a]] A frequency adjustment resistor in series with the second resistor is adjusted to position the peak gain of the band pass filter at a frequency in the range of 50 to 100 cycles/sec.

At page 3, line 25 - 35:

The input buffer is followed by an all pass phase inverter having an input coupled to receive the buffered program signal and an output that provides an inverted buffered program signal[[,]]. A band pass filter with a predetermined Q, is coupled to the buffered

program signal to provide an inverted band pass boosted program signal[[,]]. A summing amplifier adds the inverted buffered program signal to the inverted band pass boosted program signal to provide a composite program signal. A power amplifier and speaker respond to the composite program signal to [[producing]] produce an audible sound in response to the composite program signal.

At page 3, line 37 and page 4 lines 5-14:

In a more particular second embodiment[[,]] of the state-variable filter, the mid-range signal components are inverted in phase with respect to the high and low frequency signal components. [[and the]] The state-variable filter further comprises: a first amplifier stage having an inverting and non-inverting input. The program signal is coupled to the inverting input; and, a resistor divider network is coupled to the mid-range compensated signal. The resistor divider network has an output that provides a portion of the mid-range compensated signal to the first amplifier non-inverting input.

At page 5, lines 20 through 27:

The input buffer 12 is coupled to receive a program input signal at input terminal 14. The program input signal is typically received from a tape player or a CD reader. Such signals typically contain audio information such as recorded music, and have amplitudes in the range of 0 - 150 mV RMS.[[and have]] The program input signal typically has high, low and mid-range frequency audio signal components [[for providing]] that are processed by the input buffer 12 to provide a buffered program signal at terminal 16.

At page 5, lines 29 through 32:

~~The all-pass phase inverter 18 has an input coupled to receive the buffered program signal at terminal 16 and an output providing an inverted buffered program signal to terminal 20.~~

At page 5, line 34 through page 6, line 9:

The band pass filter 22 is designed to have a predetermined Q with a center frequency that is empirically selected to optimize the performance of the power amplifier 30 and speaker 38. The band pass filter 22 ~~is connected to receive the buffered program signal from terminal 16 and amplify~~ amplifies and phase invert a narrow range of low

frequency of the buffered program signal [[to provide]] and provides an inverted band pass boosted program signal to terminal 24[[,]].

At page 6, line 16 to 26:

Figure 2 is a schematic of a first embodiment of the audio boost circuit. The component values [[show]] shown were used in a circuit that was built and tested. Phantom block 12 shows the input buffer comprising a simple unity gain non-inverting amplifier. An inverting unity gain amplifier would work equally as well. The amplifier shown [[in]] is typically 1/4 of a TL072. The 10 uF capacitor is a dc blocking capacitor. The 100 pF capacitor [[is for]] provides high frequency noise suppression. A second embodiment of the input buffer using a state-variable filter is discussed later in connection with Figures 3 and 4.

At page 6, line 28 to page 7, line 9:

The all pass phase inverter within phantom block 18 is an inverting unity gain amplifier. The 100 pF capacitor is used to enhance the stability of the operational amplifier. The band pass filter within phantom block 22 is designed to have a predetermined Q in the range of from 3 to [[six]]6. The Q selected and the center frequency selected are empirically determined with the power amplifier and speaker combination for best results. The band pass filter has [[resistors]] first second and third resistors 40, 42 and 44[[.respectively]], each resistor having a first and second terminal[[,]]. The band pass filter also has a first and second capacitor[[,]] 46 and 48, [[respectively]] each capacitor having a first and second terminal. Operational amplifier 50 has an inverting input, a non-inverting input and an output connected to terminal 24. The non-inverting input is connected to a reference potential such as ground.

At page 7, line 17 to page 7 line 26:

The second resistor 42 second terminal is connected to the first terminal of resistor 56~~a reference potential such as ground~~. In the embodiment of Figure 2, adjustable resistor 54 is connected in parallel with resistor 56, the pair being [[and the pair are]] in series with resistor 42 to form a frequency adjustment means for adjusting the frequency at which the peak gain of the band pass filter 22 occurs. The adjustment means could be a single equivalent value resistor selected to replace the second resistor 42 in series with the parallel combination of the adjustable resistor 54 and resistor 56.

At page 7, line 28 through page 7 line 33:

The first capacitor 46 second terminal is connected to the inverting input of operational amplifier 50 [[operational amplifier's inverting input]] and to the third resistor's 44 first terminal. The second terminal of capacitor 48 is connected to the output terminal 24 of operational amplifier 50 and to the second terminal of the third resistor 44 ~~capacitor's 48 second terminal is connected to the operational amplifier's output terminal and to the third resistor's 44 second terminal~~.

At page 8, line 20 through line 32:

However, the topology for a set of design requirements is not unique nor are the values for a given topology. The following example and equations show how the component values are determined for [[an]] a circuit in which the Q, center frequency f and the peak gain Ao are given. In general, the Q of a band-pass filter is defined as the bandwidth divided by the center frequency. Assume that the center frequency required is 78.8 Hz. Assume that the Q required is 5.4 and the peak gain Ao required is 1.03. The first and second capacitors have the same value which is defined as c. A convenient value of 0.39 uF is selected for a first try. Using the design procedure found in the "Handbook Of Operational Amplifiers Active RC Networks" mentioned above:

At page 10, lines 10 - 17:

The values of R1, R2 and R3 [[corresponds]] correspond to the values of the first, second and third resistors in the previous example. It can be seen that the values of resistors are obtainable for the range of Q of 3 to 6 that is desired. The frequency adjustment resistor 54 and the values of resistors 42 and 56 which combine to form R2 in the calculations above are calculated or determined empirically to position the peak gain at a frequency in the range of 50 to 100 [[herts]] hertz.

At page 10, line 19 to 26 and page 11. lines 5 - 7:

The summing amplifier within phantom block 26 represents a means for adding the inverted buffered program signal to the inverted band pass boosted program signal and for providing a composite program signal. Resistor 58 has a first and second terminal. The first terminal of resistor 58 is connected to terminal 20 to receive the inverted buffered program signal. The second terminal of resistor 58 is connected to the inverting input of operational amplifier 59 and to the first terminal of the feed-back resistor 62. The second

terminal of the feedback resistor 62 is connected to the output of the summing amplifier terminal [[28]]26.

At page 11, lines 9 - 18:

Resistor 64 and 66 in series have a first and second terminal. The first terminal of the series combination is connected to terminal 24 to receive the inverted band pass boosted [[buffered]] program signal. The second terminal of the series combination is [[also]] connected to the inverting input of the operational amplifier 59 in summing amplifier 26 and to the first terminal of the feed-back resistor 62. ~~The first terminal of the series combination is connected to terminal 24 to receive the inverted band pass boosted program signal from the band pass filter.~~

At page 11, line 26 through page 11 line 34:

Figure 3 is shows the block diagram of a second alternative embodiment of the input buffer 12 using a state-variable filter 72 responsive to the program input signal at terminal 14 for separating and processing the [[having]] high, low and mid-range frequency signal components of the program signal. This second embodiment of the input buffer 12 has ~~a state-variable filter 72 and~~ a state-variable summing amplifier 74 for adding the high, low and mid-range frequency signal components to provide the buffered program signal at terminal 16.

At page 11, line 37 and page 12 lines 5 - 10:

The state-variable filter 72 has a first amplifier stage 90 responsive to the program signal for providing a high frequency compensated signal Vhp; a second amplifier stage 98 responsive to an output of the first amplifier stage for providing a mid-range compensated signal Vmp; and a third amplifier stage 104 responsive to the mid range compensated signal for providing a low range compensated signal Vlp.

At page 12, lines 12 - 26:

In Figure 4, the input buffer 12 has gain control circuitry within the state-variable summing amplifier 74, such as adjustable resistors 114, 115 and 116, for balancing and summing the high, low and mid-range frequency compensated signals.

The state-variable filter within phantom box 72 is coupled or connected to the program input signal at terminal 14 and processes the program input signal into high, Vhp,

low , Vlp and mid-range, Vmp frequency compensated signal components. The state-variable summing circuit 74 adds the high frequency compensated signal, the low frequency compensated signal and the mid-range frequency compensated signal to provide the buffered program signal at terminal 16. Adjustable resistors 114 and 116 represent ~~The input buffer also provides~~ an adjusting means within the state-variable summing amplifier 74 for adjusting the gain between the high and low frequency compensated [[signal]] signals and the mid-range signal.

At page 12, line 28 through page 12 line 37:

~~The three band-pass signals comprise a low band-pass signal Vlp (a low-range compensated signal) on signal line 76, a mid-range bandpass signal Vmp (a mid-range compensated signal) on signal line 78 and a high range bandpass signal, Vhp (a high frequency compensated signal) on signal line 80 to respective inputs of a state-variable summing amplifier 74.~~ The mid-range frequency compensated signal, Vmp [[components]] produced by the state-variable filter 72 [[are]] is inverted in phase with respect to the phase of the high and low frequency compensated signal components produced by the state-variable filter 72.

At page 13, line 22 through 31:

Referring again to Figures 3 and 4, phantom block 90 represents an input summing and damping amplifier circuit. The program input signal at terminal 12 and the low range frequency compensated [[bandpass]] signal Vlp on signal line 76 are fed to the inverting input of amplifier 92. A portion of the mid-range frequency compensated [[band-pass]] signal Vmp is fed to the non-inverting input of amplifier 92 for damping via the damping input 94. The [[resulting]] output of amplifier 92 [[was]] is the high frequency compensated signal [[component]] Vhp at amplifier output 96 which [[was]] is connected to signal line 80[[,]].

At page 13, line 33 through line 37:

The high frequency compensated [[range band-pass]] signal Vhp is [[then]] also connected to the negative input of a first integrator shown within phantom block, for inversion and integration and to the state-variable summing amplifier 74 high pass input 100 on signal line 80.

At page 14, line 5 through line 10:

The first integrator 98 integrates the Vhp signal to provide the mid-range frequency compensated [[band-pass]] signal Vmp at first integrator output 102. The mid-range frequency compensated [[band-pass]] signal Vmp is fed to the damping input 94 of the input summing and damping amplifier circuit 90 and to the state-variable summing amplifier 92 mid-range frequency compensated signal [[band-pass]] input 86 on signal line 78.

At page 14, line 12 through line 19:

Phantom block 104 represents a second integrator that responds to the mid-range frequency compensated [[bandpass]] signal Vmp on signal line 78 and provides a low bandpass signal Vlp at the second integrator output terminal 106 to the state-variable summing amplifier 74 low range frequency compensated [[band-pass]] signal input 84 via signal line 76. The low frequency compensated [[bandpass]] signal Vlp is also fed to a second input 108 of the input summing and damping amplifier circuit 90.

At page 14, line 21 through page 14 line 34:

The damping circuit of the input summing and damping amplifier circuit 90 comprises an input resistor 110 that has a first terminal connected to receive the mid-range frequency compensated [[band-pass]] signal, Vmp, at damping input 94. The second terminal of resistor 110 is coupled to the first terminal of resistor 112 and to the non-inverting input of operational amplifier 92. The second terminal of resistor 112 is coupled to a reference potential such as ground. The ratio of resistors 110 and 112 establish the "Q" of the state-variable filter. The higher [[the gain, of]] the ratio of the resistors 110 and 112, the higher the Q. The Q of the state-variable filter of Figures 3 and 4 is typically in the range of 0.5 to 2 for audio applications. The Q of the circuit of Figure 4 is approximately 0.67.

At page 14, line 36 to page 15 line9

One of the objectives of the state-variable filter 72 is to set phase shift and gains up such that the mid-range frequency compensated [[band-pass frequency]] signals are about 180 degrees out of phase with the signal components in the lower frequency band and in the higher frequency band. The ratio of the damping resistors, the gains and break frequencies of the amplifiers and integrator are set for a desired Q and bandpass.

At page 15, line 11 through line 17:

The state variable summing amplifier 74 has a low frequency band-pass gain adjustment pot 114, and a high range band-pass frequency gain adjustment pot 116 that permit the user to make a final adjustment for a particular circuit and component configuration. The adjustable inputs to the state variable summing amplifier 74 permit the user to obtain additional gain control of [[for]] the Vhp and Vlp [[signal]] signals.

At page 15, line 37 through page 16 line 10:

Referring again to Figure 4, a reactance chart check will show that the break frequency for the mid-range bandpass amplifier 98 [[to be]] is about 2.24 KHz. The break frequency for the low range bandpass amplifier 104 is about a decade lower at 224 Hz at three dB per octave. The Q of the circuit of Figure 4 is approximated by the following equation:

At page 16, 25 through page 16 line 32:

~~In general, the Q of a band-pass filter is defined as the bandwidth divided by the center frequency.~~ The design of the state variable filter of Figure 4 is taught in the text "The Active Filter Handbook" by Frank P. Tedeschi, pg 178 - 182, Tab Books Inc of Blue Ridge Summit, Pa., 17214; however, this reference does not show the outputs being summed to form the desired unbalanced output that meets the desired requirement for audio applications.

At page 16, line 34 through page 17, line 30:

The object of the design of Figure 4 is to have a first break frequency at approximately 240 Hz and a second at 2.24 KHz, about a decade away from the first break. The low break fc is established by the equation:

$$fc = 1/2\pi RC2$$

where R and C are the value of resistor [[116]]113 and capacitor [[118]]117 . The high frequency break is set by the

$$fc = 1/2\pi RC1$$

where the value of R and C1 are those of resistor 120 and capacitor 122.

Once the Q is selected, the ratio of R1 to R2 can be calculated from the equation. In the case of Figure 4, a Q of 0.67 was selected by knowing what the desired gain bandwidth response curve would be from the above referenced

U.S. Patent 4,638,258. The circuit was modeled using a computer aided analysis program such as SPICE. The break frequencies were estimated from the information in the referenced U.S. Patent 4,638,258. Initial component values were selected based on available components. A reactance chart can be used for a quick approximation of the required remaining value once one of the values are known. The circuit shown had [[an initial]] a goal of a design [[a]] center frequency at 700 Hz. At the center frequency, the gain of the circuit is about -1 dB or less than 1. The two adjustment pots, [[116 and 114]] 114 and 116 permit an adjustment of the gain of the Vlp and the Vhp by about 15 dB with the values shown.

At page 17, line 32 through page 18 line 6:

The Q [[was then]] is adjusted using the pots 114 and 116 to provide [[the]] a best match to the curves in the earlier patent to Crook. The Q and the break points were selected to match the response characteristic of the resulting circuit to the curves in the earlier patent to yield the same phase shifts, time delays and frequency response. [[The resistors]] Resistors 114 and 116 are set for a gain of nine but a slightly higher gain of 12 [[would be]] is preferred.

At page 18, line 17 through line 24:

The procedure for adjusting the band-pass and gain as proposed in the above referenced text "The Active Filter Handbook" by Frank P. Tedeschi, at pages 178 - 182" is to set the value of C1 and C2 to be equal and to adjust the ratio of R1 and R2 and to obtain the desired Q. In ~~the circuit of Figure 4, the~~ state-variable summing amplifier 74, the gain controls for the Vhp and Vlp signals provide for independent control of the gain and band-pass.